REMARKS

The Office Action of November 19, 2005, has been carefully reviewed and these remarks are responsive thereto. Claims 47, 48, 50, 55, 56 and 57 have been amended. Claims 47 – 60, 62, 63, 65 and 66 remain pending. Reconsideration and allowance of the instant application are respectfully requested.

Rejection of the Claims Over Hemink et al.

Claims 47-60, 62, 63, and 65-66 stand rejected under 35 USC § 102(a) over Hemink et al. Applicants traverse.

Claim 47 recites:

> " a first string line including a first memory cell and a first select transistor connected in series;
>
> ...
>
> a first bit line connected to said first string line ...
>
> a common latch circuit having a common node connected to one ends of said first and second bit lines..."

Claim 47 has been amended to clarify that the NAND series and bit line are different. The NAND series is the "string line". The bit line is different from the "string line". Hemink et al. shows only the NAND series of Figure 8 with no separate bit line as claimed. Further, in Figs. 8, 13 and 20 of Hemink et al., bit lines are not connected to a common node of a common latch circuit as is now claimed.

Accordingly, as now claim 47 recites that the "string line" and the "bit line" are two different elements, the claim is allowable over Hemink et al.

Claims 48, 50, 55, 56 and 57 have been similarly amended and are believed allowable.

Dependent claims 49, 51-54, 58-60, 63, and 65-66 are believed allowable as they depend on allowable independent claims.

Rejection of the Claims Over Sakui

Claims 47-60, 62, 63, and 65-66 stand rejected under 35 U.S.C. § 102(e) over Sakui.

Claim 47 recites:

> " a first string line including a first memory cell and a first select transistor connected in series;
>
> a second string line including a second memory cell and a second select transistor connected in series;
>
> a first bit line connected to said first string line;
>
> a second bit line connected to said second string line, being different from said first bit line; and
>
> a common latch circuit having a common node connected to one ends of said first and second bit lines…"

With respect to Figure 38 of Sakui, a node of a latch circuit to which a bit line BLi is connected is different from a node of a latch circuit to which a bit line /BLi is connected. In other words, Sakui is the same as Hemink et al. in the point that bit lines are not connected to a common node of a common latch circuit as claimed.

As Sakui fails to disclose each and every feature of claim 47, the claim is allowable over Sakui.

Claims 48, 50, 55, 56 and 57 have been similarly amended and are believed allowable.

Dependent claims 49, 51-54, 58-60, 63, and 65-66 are believed allowable as they depend on allowable independent claims.

If any fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733 accordingly.

Respectfully Submitted,

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